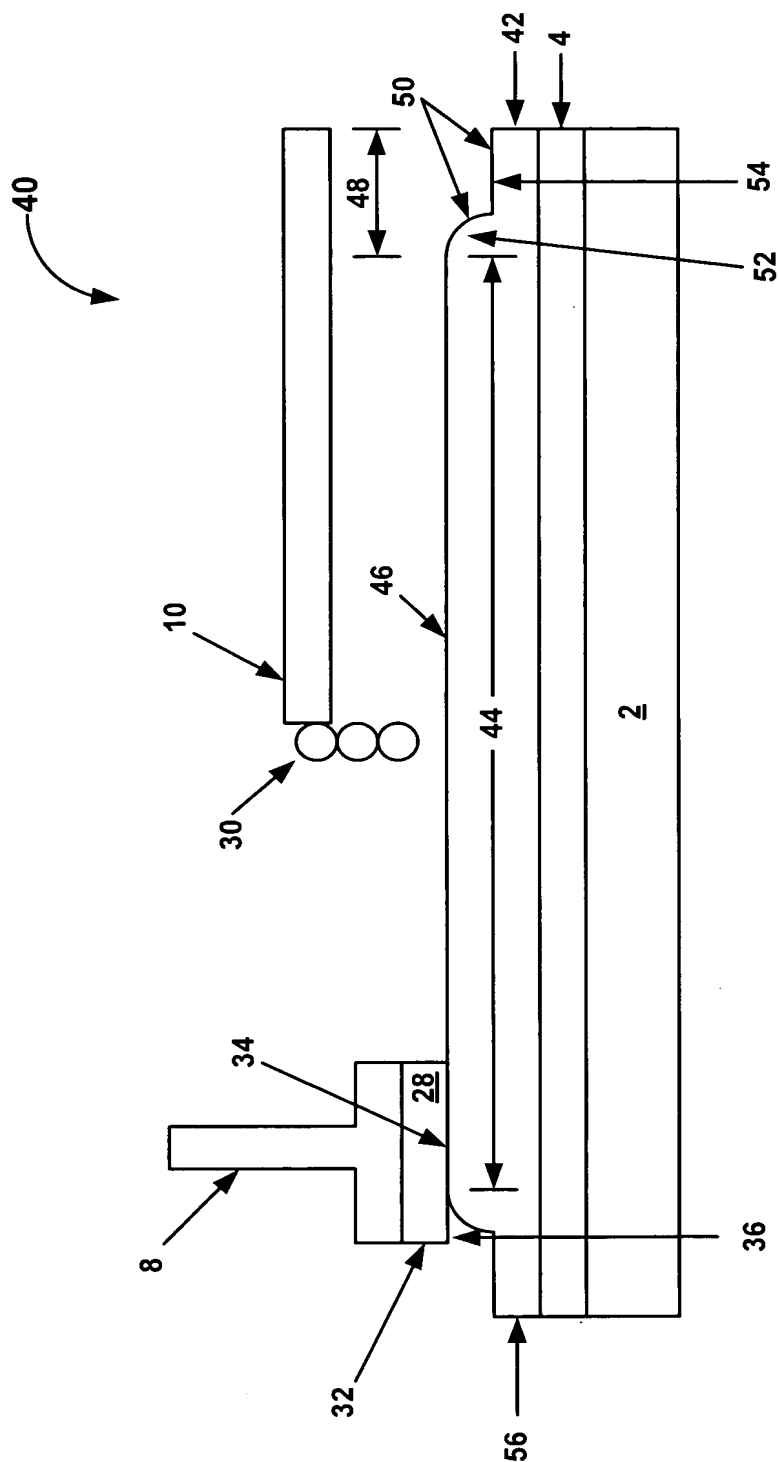


FIG. 2



FIG. 3





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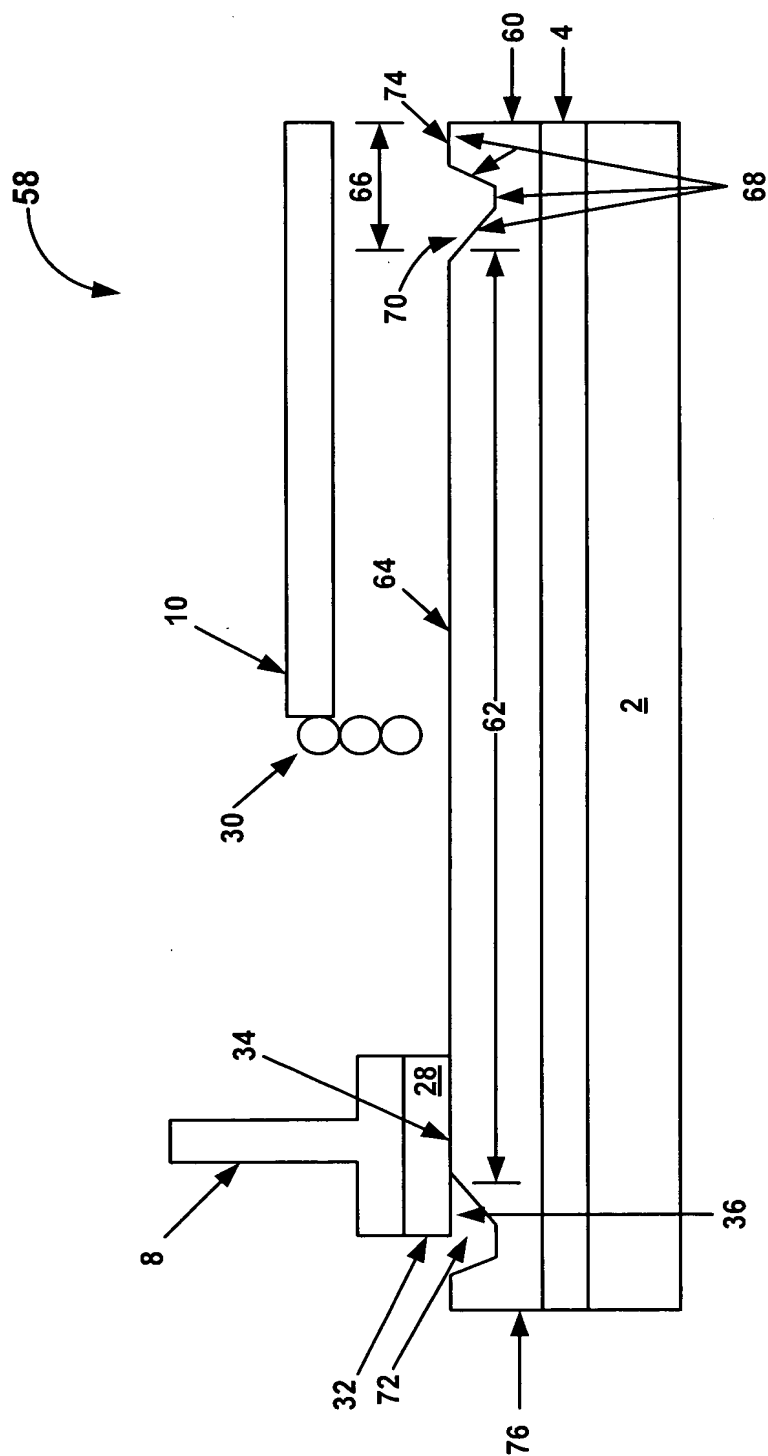


FIG. 4

A cross-sectional diagram of a semiconductor device assembly. A substrate 8 has a central layer 72 and side regions 32. On top of the central layer is a gate stack 28, which includes a gate dielectric 34 and a gate electrode 8. To the left of the gate stack is a contact pad 10 connected to the side region 32 via a contact plug 30. To the right of the gate stack is another contact pad 90 connected to the side region 72 via a contact plug 86. The entire assembly is covered by a passivation layer 80, which has a thickness dimensioned as 4. A reference numeral 78 points to the overall assembly. Other labels include 2, 36, and 92, which likely refer to other views or components of the device.

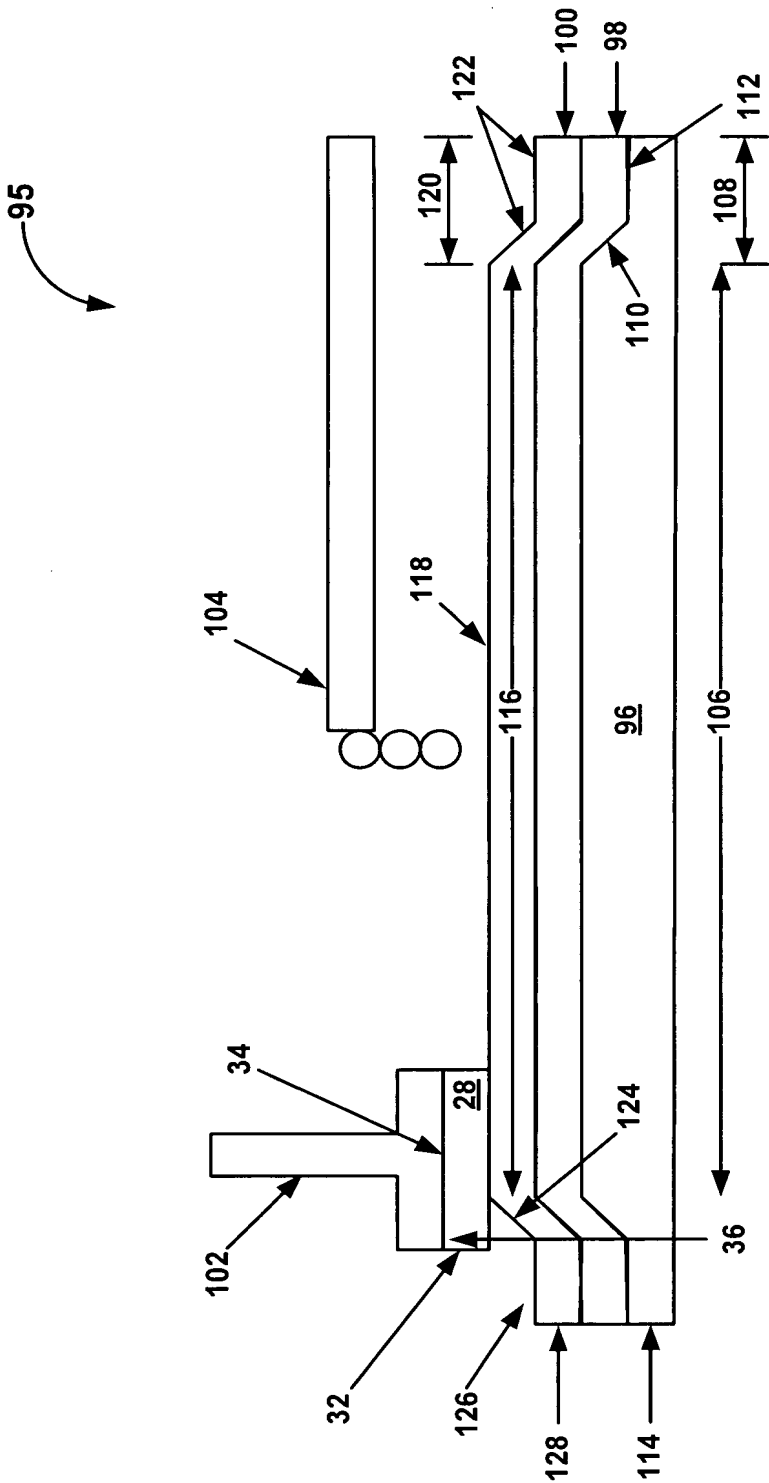


FIG. 6

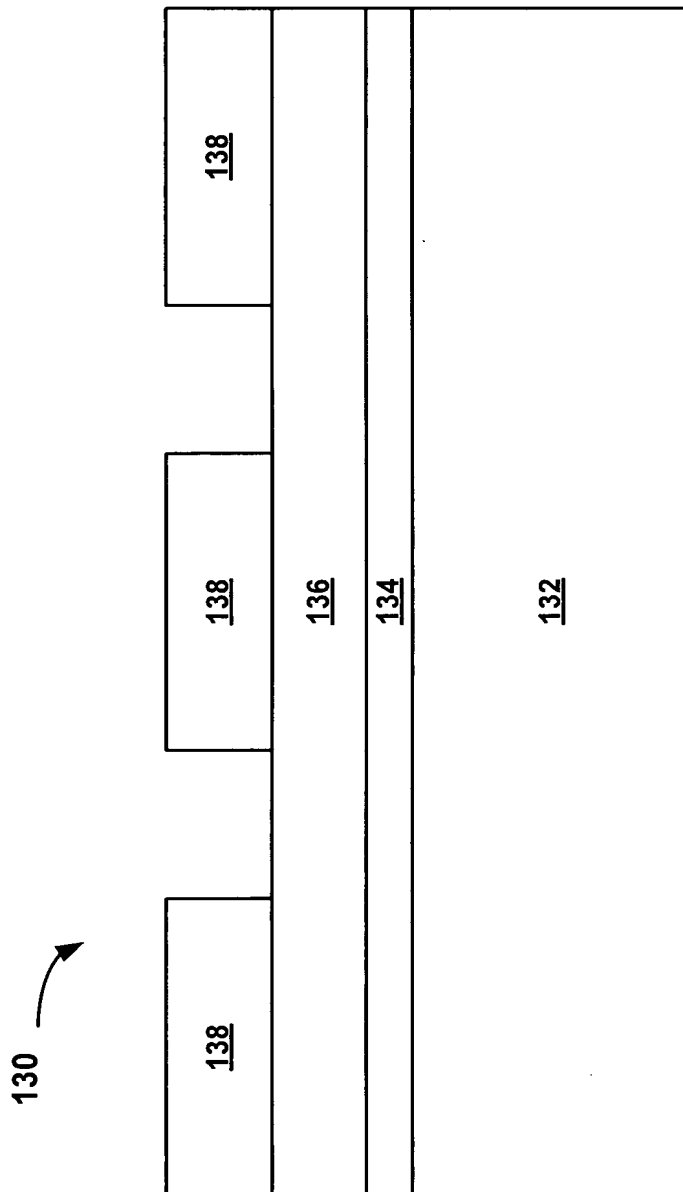


FIG. 7

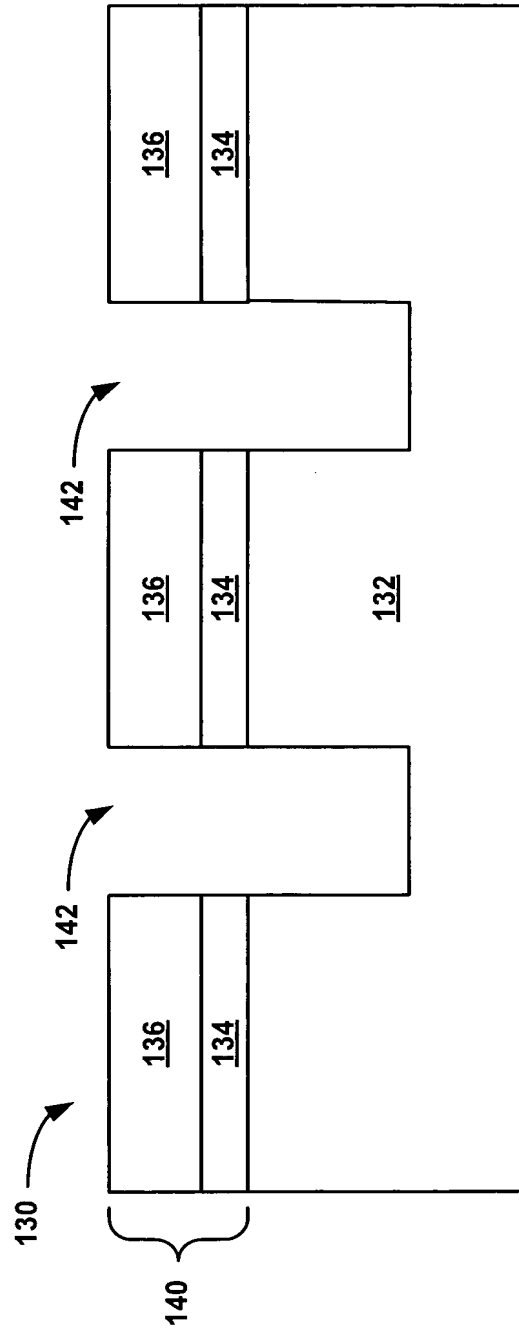


FIG. 8

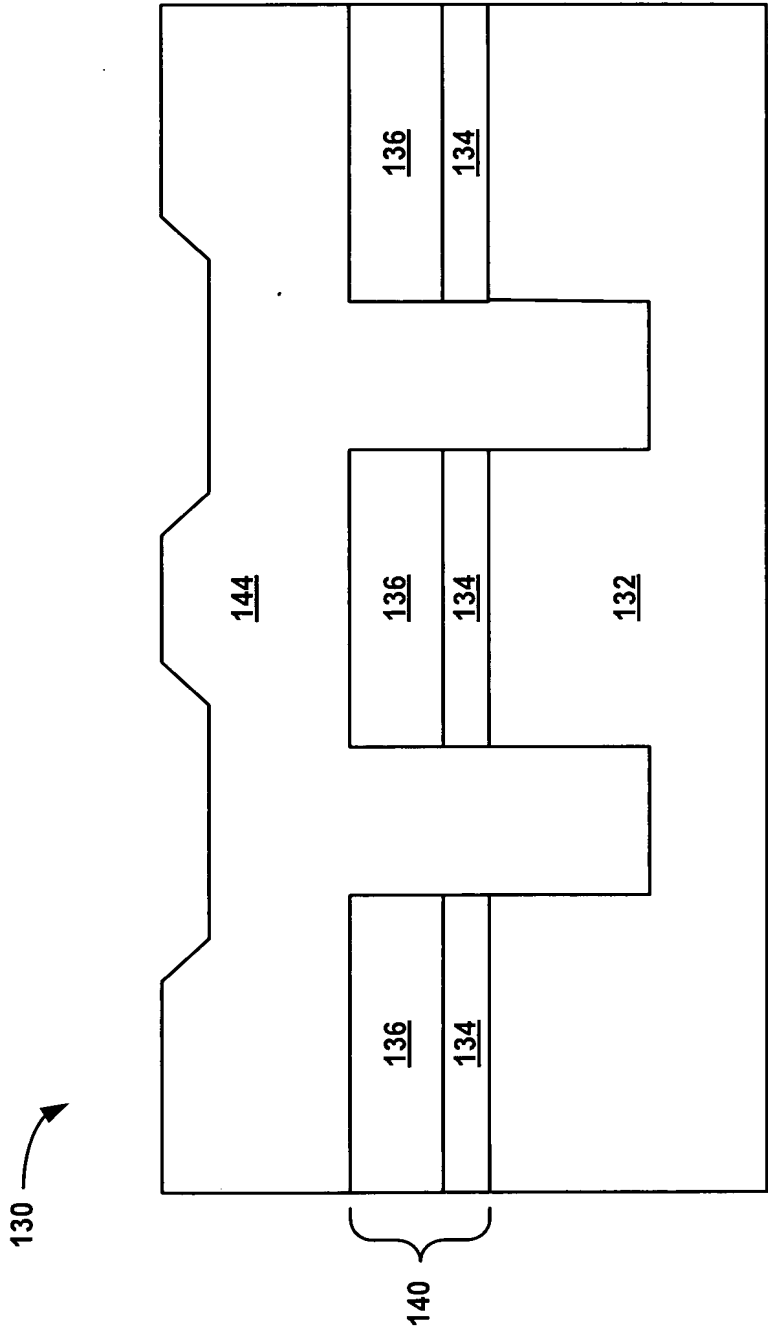


FIG. 9



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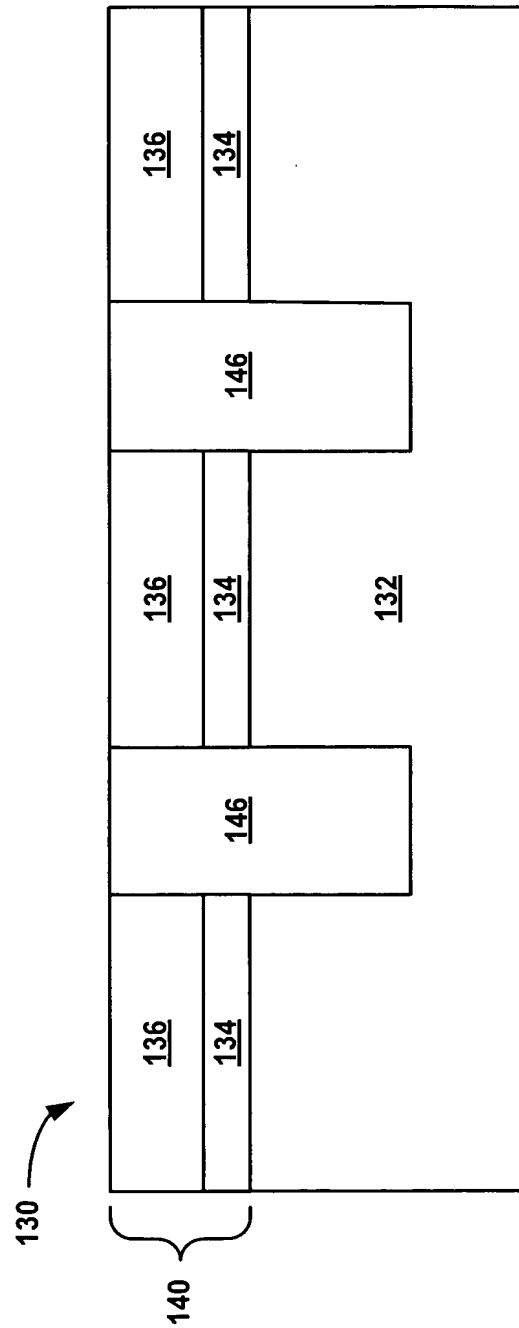


FIG. 10



TITLE: POLISHING APPARATUS AND METHOD FOR FORMING AN INTEGRATED CIRCUIT
INVENTOR(S): Feng Chen, Charles Lin, Lup San Leong Attorney Docket #: CHRT-99203.DIV

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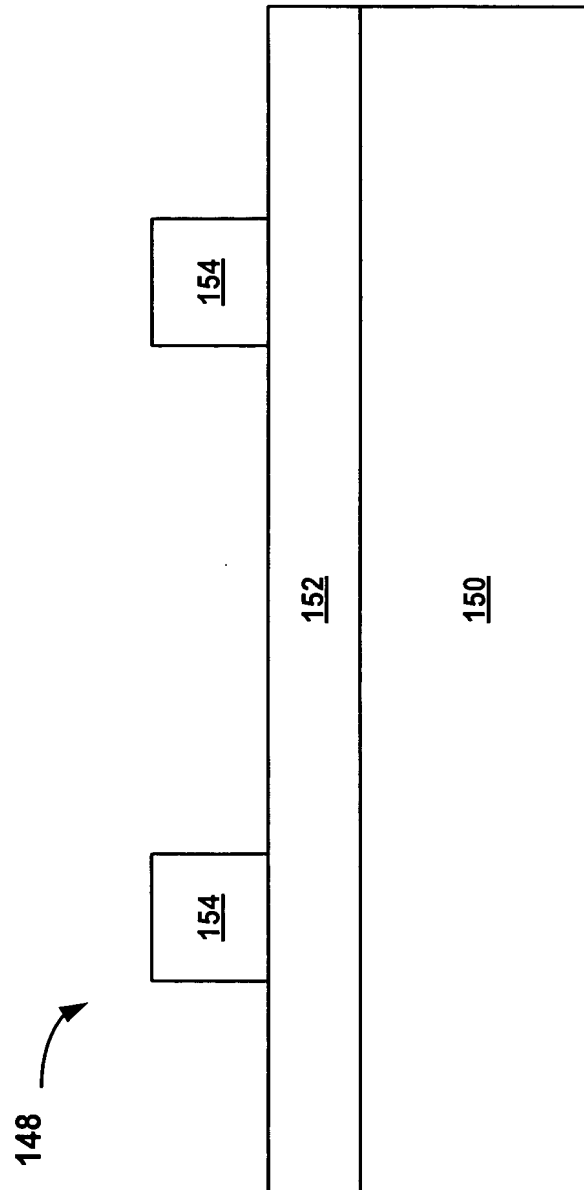


FIG. 11

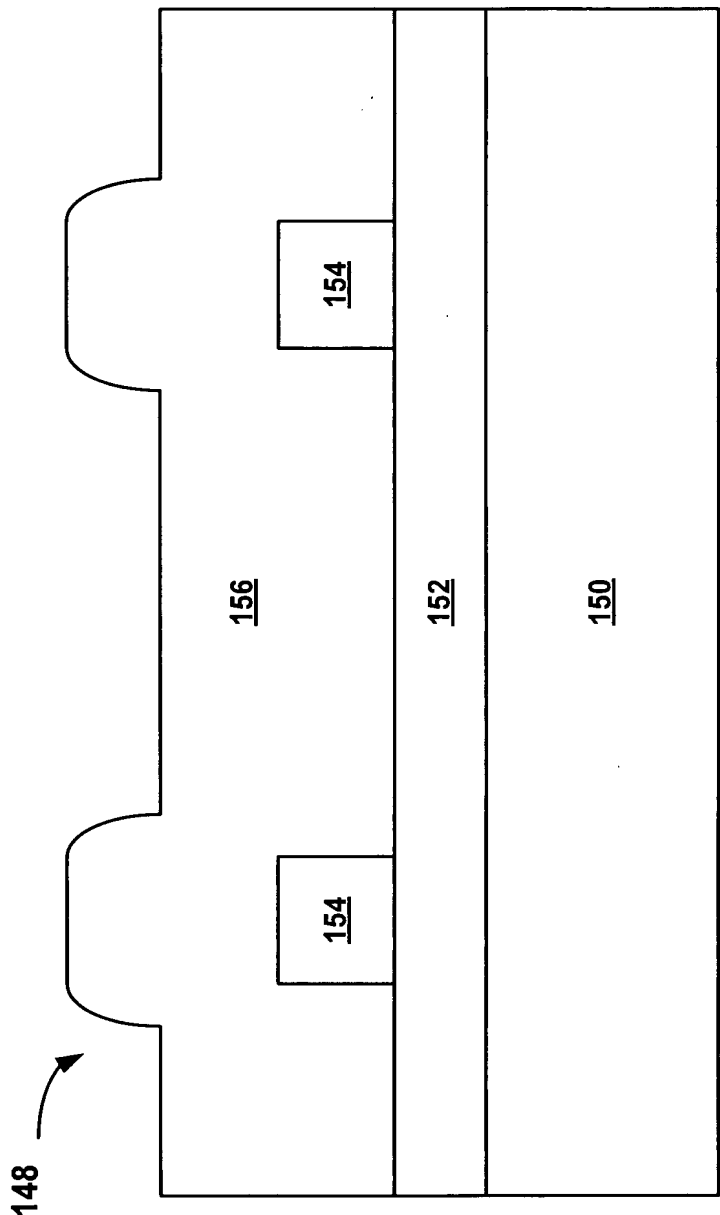


FIG. 12

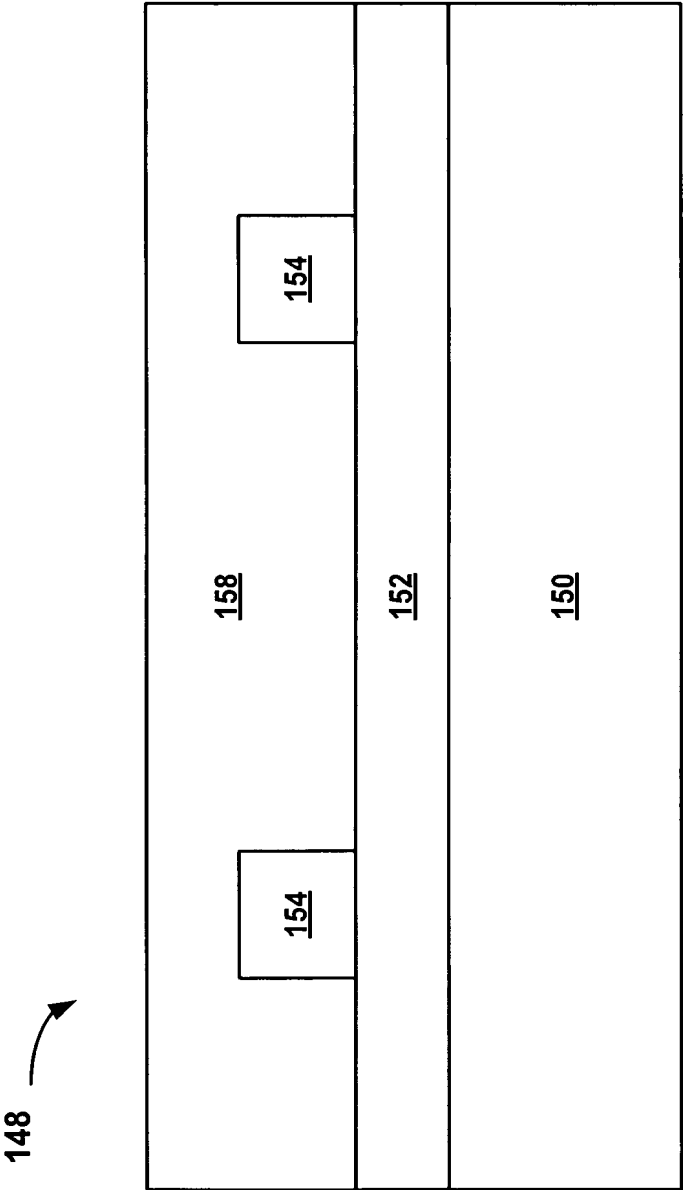
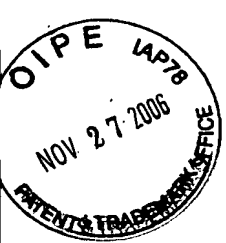


FIG. 13

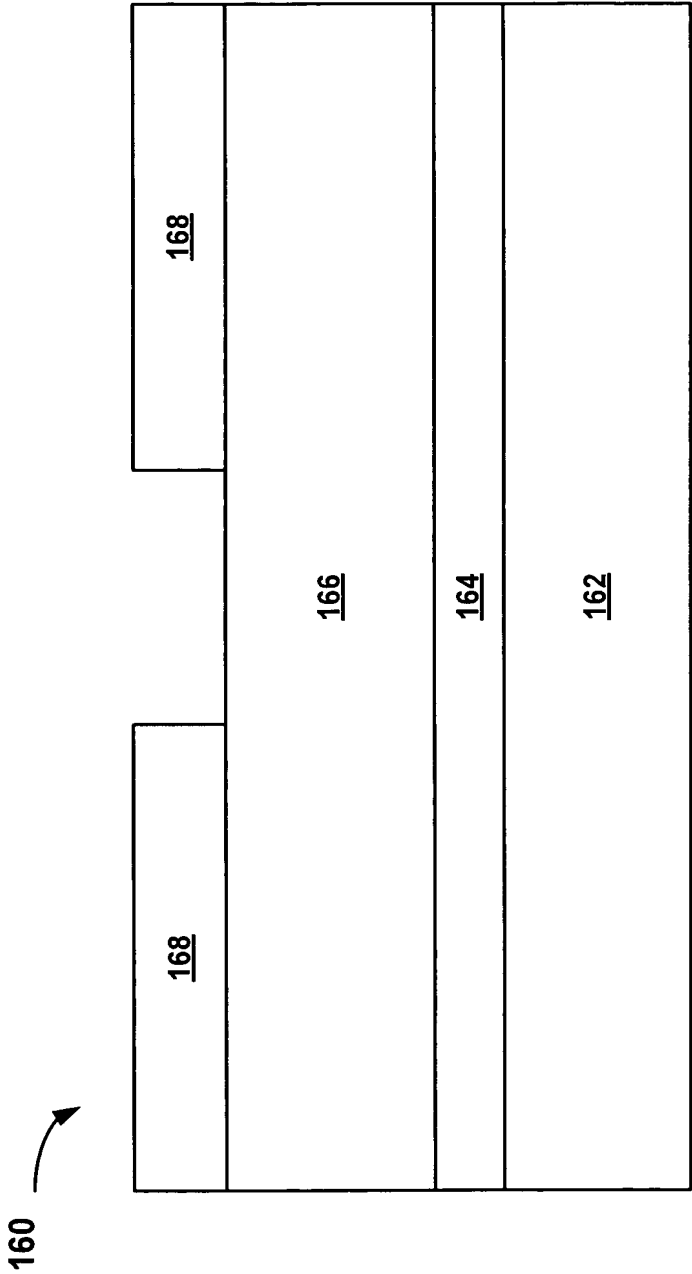


FIG. 14

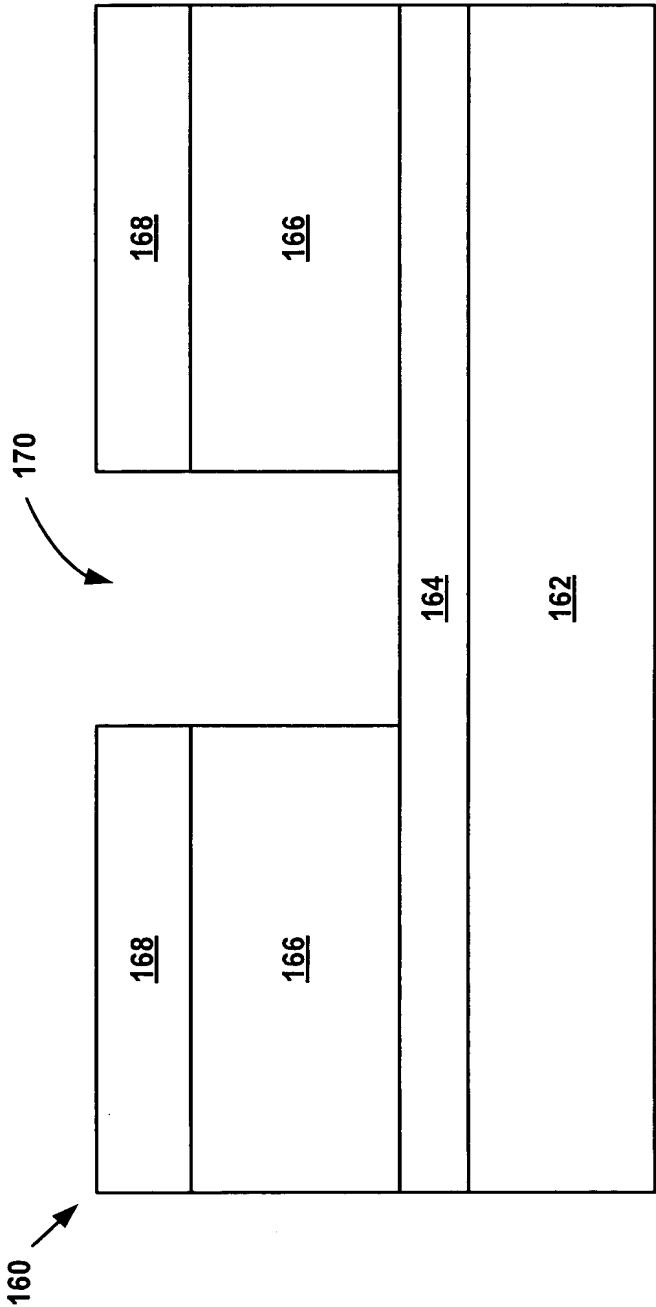


FIG. 15

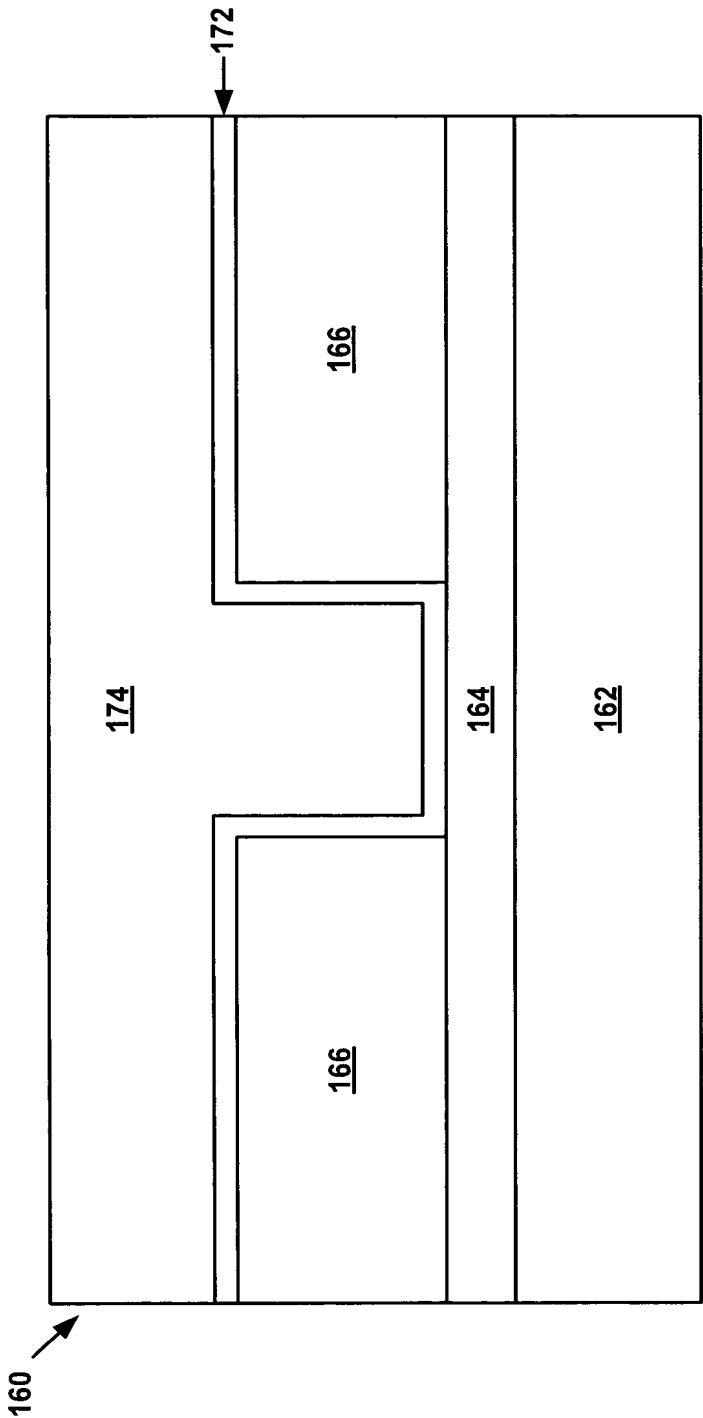


FIG. 16



TITLE: POLISHING APPARATUS AND METHOD FOR FORMING AN INTEGRATED CIRCUIT
INVENTOR(S): Feng Chen, Charles Lin, Lup San Leong Attorney Docket #: CHRT-99203.DIV

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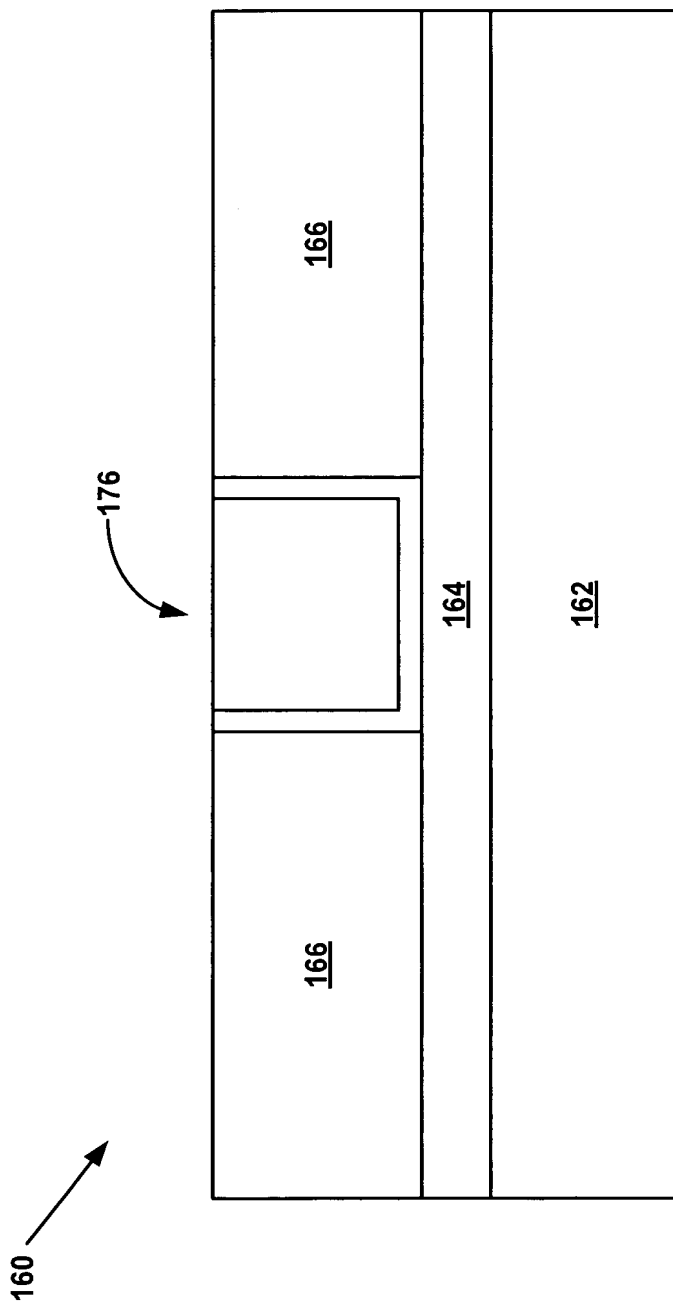


FIG. 17